Room-Temperature Quantum Confinement Effects in Transport Properties of Ultrathin Si Nanowire Field-Effect Transistors

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ABSTRACT: Quantum confinement of carriers has a substantial impact on nanoscale device operations. We present electrical transport analysis for lithographically fabricated sub-5 nm thick Si nanowire field-effect transistors and show that confinement-induced quantum oscillations prevail at 300 K. Our results discern the basis of recent observations of performance enhancement in ultrathin Si nanowire field-effect transistors and provide direct experimental evidence for theoretical predictions of enhanced carrier mobility in strongly confined nanowire devices.

KEYWORDS: Quantum confinement effects, Si nanowires, room-temperature quantum oscillations, top-down patterning, ultrathin Si nanowire transistor

Quantum confinement of carriers has an extensive influence on the physics of nanoscale device operation. However, experimental study of quantum confinement effects was mostly limited to ultralow temperatures until recent years due to relatively large channel diameters of devices. For practical applications of quantum characteristics, it is crucial for such effects to manifest at room temperature, which naturally dictates the size of the channel be reduced well into single-digit nanometer range so that the quantum size effect is able to overcome thermal broadening. In recent years, quantum oscillatory behavior has been reported to persist at elevated temperatures in one-dimensional (1D) devices with reduced dimensions. There has been considerable effort to improve key device parameters such as transfer conductance and carrier mobility of such narrow Si nanowire (SiNW) devices.

More recently, it has been possible to lithographically (top-down) fabricated SiNW FETs on silicon-on-insulator (SOI) substrates with device diameters as small as 3 nm, and significant performance enhancement has been reported at 300 K in top-down patterned sub-5 nm p-Si NW FETs. Here, we demonstrate quantum confinement effect in transport properties of ultrathin p-Si FETs at room temperature. Clear plateau-like structures in drain–source current (I_D) are revealed in the subthreshold region of sub-5 nm p-SiNW FETs at 300 K. Oscillations in both transconductance (g_M) and channel conductance (g_D) are analyzed with respect to quantum confinement-induced subband structure. The genuine oscillatory behaviors of conductance and carrier mobility are understood in terms of strong confinement of carriers in quantized 1D subband structure with corresponding unique 1D density of states (DOS). We compile the findings of our study into a framework to present clear experimental evidence of measurable quantum confinement effects (at 300 K) and also justify the recently reported enhanced carrier mobility in sub-5 nm SiNW FETs at room temperature.
**Method.** To demonstrate quantum size effects at room temperature, we fabricated sub-5 nm thick Si[110] NW FETs lithographically on a SOI substrate, and performed high-resolution transmission electron microscopy (HR-TEM) imaging to confirm dimensions and uniformity of channel bodies in measured devices. Figure 1 shows a three-dimensional (3D) schematics of the device and HR-TEM images of the cross section of a nanowire body before (a) and after (b) thermal oxidation. All electrical transport measurements were performed in air at room temperature using a shielded probe station with triax connectors in order to minimize RF radiation noise. (See more details of SiNW device fabrication and transport measurements in ref 11.) After electrical characterization, cross section of each device was prepared with focused ion beam and imaged by HR-TEM to measure dimensions and examine morphology. Cross sections of the SiNWs showed a single-crystalline surface having a nearly circular and smooth profile with dimensions as low as 3 nm. (See ref 11 for additional HR-TEM images and interfacial details.) In these SiNW FETs, two bias fields are provided from external sources: the transverse gate voltage applied to the back-gate electrode $V_{BG}$ determines the effective width of the channel and the longitudinal drain–source voltage $V_{DS}$ transports carriers through the channel body.

**Quantum Confinement in 1D SiNW FETs.** First, we identify quantum size effects in transfer characteristics of p-SiNW FETs. As illustrated in Figure 1, the channel body of ultrathin SiNW FETs is confined in both [001] (top) and [110] (sides) directions, so that motion normal to [110] is restricted physically by the SiNW channel body and the carriers (holes) are free to move only in the [001] direction, producing a series of quantized energy levels; each energy level forms a subband. Subband energies and hence intersubband structure depend strongly on the boundary conditions of quantum confinement, which is closely related to the cross sectional shape of NWs. Each sub-5 nm SiNW essentially forms a 1D system of electrons, since the diameter of the NWs is close to the wavelength of an electron ($\sim 10$ nm). The corresponding 1D subband structure results in a series of sawtooth-like oscillatory DOS.\(^1\)\(^3\)\(^4\)\(^5\) (See Figure S1 in Supporting Information.)

As shown in Figure 2, the source–drain current $I_{DS}$ increases quasi-linearly at low back-gate voltage $|V_{BG}|$. However, when $|V_{BG}|$ is increased further, the channel current starts to increase superlinearly and several steplike and oscillatory structures are observed in drain current and transconductance, respectively. Clear shoulders or steplike structures are visible in drain current $I_{DS}$ of the SiNW FET at 300 K. The nanowire has a cross section of 4.3 nm $\times$ 5.1 nm. The inset shows characteristics of a Si nanobelt (SiNB) FET with a cross section of 4.3 nm $\times$ 161 nm for comparison. The data are of p-MOS devices; the horizontal axis is shown as a magnitude of back-gate voltage for convenience.

![Figure 1. Schematics of SiNW device and HR-TEM image. Three-dimensional schematic of a back-gated SiNW FET patterned on a silicon-on-insulator (SOI) substrate of buried oxide (BOX) and a HR-TEM image of an oxidized Si[110] NW channel body cross section before (a) and after (b) thermal oxidation.](image)

![Figure 2. Drain current and transconductance characteristics of a SiNW FET at 300 K. The nanowire has a cross section of 4.3 nm $\times$ 5.1 nm. The inset shows characteristics of a Si nanobelt (SiNB) FET with a cross section of 4.3 nm $\times$ 161 nm for comparison. The data are of p-MOS devices; the horizontal axis is shown as a magnitude of back-gate voltage for convenience.](image)
current spectrum shown in Figure 2 indicates that near-threshold carrier conduction (|V_BG| ~ few volts) occurs through several subband channels.

Transfer characteristics of NW FETs with very dissimilar cross sectional profile would be different, since quantum confinement effects are closely related to channel boundary conditions. (See Figures S2–S4 in Supporting Information for more on transfer characteristics.) The dissimilarity between the transconductance characteristics of Si-FETs patterned with a NW (Figure 2) versus a NB (inset of Figure 2) is physically plausible, recalling features in the DOS of the 1D versus 2D structures. A Si FET consisting of a NW with a cross section of 4.3 nm × 3.6 nm is essentially a 1D system with a sawtooth like DOS but that of a NB with cross section of 4.3 nm × 161 nm is a quasi-2D system with stairlike DOS. (See Supporting Information Figure S1 for the DOS.) Carrier confinement and the corresponding DOS can result in oscillations in carrier conductance and mobility. The transfer characteristics of the NB FET (inset of Figure 2) show fast increase of I_DS with gate voltage, while g_m shows uniformly increasing conductance peaks with larger interpeak separation, which is an indication of the ladderlike 2D DOS profile resulting from the accumulated contributions of individual 2D subband channels. Instead, the characteristics of the NW FET reveal relatively quick current saturation accompanied with reduction of g_m for increasing gate bias, implying behavior of inverse-square-root singular 1D DOS at the bottom of each 1D subband. We also note that geometrically narrower dimensions of “cylindrical” NWs result in both nonuniformly spaced and larger subband separations, but laterally confined NBs resemble a quasi-2D electron gas of uniformly spaced subband structure (with increasing separations for higher subbands).

**Channel Conductance Behavior and Intersubband Spectroscopy.** Here, we identify quantum size effects in channel conductance characteristics and related intersubband separations in p-SiNW FETs. For a given value of V_BG, the channel conductance, g_0 (= δI_DS/δV_DS|V_BG=const.), also varies with V_DS. (See Figure S5 in Supporting Information.) The periods of repeated structures in I_DS can be obtained by analyzing g_0 in terms of V_DS and 1D intersubband separation can be determined from the g_0 characteristics with V_DS. Figure 3a shows a contour representation of d_g_0/dV_BG at 300 K, as functions of V_DS and V_BG. Patterns of strong oscillations in d_g_0/dV_BG are clearly visible. The dark (blue) areas refer to the regions of quickly increasing channel conductance, while light (green) areas represent the regions of quickly decreasing channel conductance. The zero and high values of d_g_0/dV_BG correspond to conductance plateaus and interplateau transition regions in I_DS−V_DS curve. Figure 3b illustrates measured I_DS−V_DS characteristics of a p-SiNW FET for various values of V_BG at 300 K and corresponding g_0−V_DS (curves for V_BG = −0.3 and −0.9 V shown). Strong oscillations in g_0 with both biases V_DS and V_BG are clearly seen with amplitude of oscillations increasing at higher values of V_DS and V_BG. For I_DS−V_DS curves, the V_BG is changed in −0.2 V steps and the lowest trace in the figure is for V_BG = −0.3. V. In general, I_DS increases with V_DS and V_BG, because the energy states for current flow and the number of 1D conduction channels increase, and g_0 shows strong oscillation with increasing V_DS. In Figure 3b, stairlike increase in I_DS(V_DS) is seen, and we find that the peaks in g_0 are nearly uniformly spaced. It is also apparent that the period of g_0 increases slightly as the magnitude of back-gate voltage V_BG increases, implying that a higher gate field gives rise to further confinement of the carriers in the channel body, leading to increased separation between subbands; the transverse gate field induces further confinement (“field-induced confinement”) of the carriers in the narrow channel body. From the g_0−V_DS curves at a given V_BG, the subband separation ΔE_{n+1,0} can be extracted. (See Supporting Information Text S.) Let us consider the case of the equilibrium chemical potential μ_0 (= E_F) located somewhere between subband energies E_n and E_{n+1}. (See Supporting Information Figure S1.) As V_DS is increased slowly, I_DS remains constant staying on the same plateau, waiting until either μ_0 gets equal to E_{n+1} (V_DS) or μ_0 equal to E_n (V_DS) at V_DS so that a new subband channel opens and I_DS increases to a new value I’_DS. On increasing V_DS, extrema in g_0(V_DS) can occur at characteristic values of V_DS. If we let the two nearest maxima of g_0(V_DS) occur at the drain voltages V_1 and V_2 the corresponding intersubband separation is given by ΔE_{n+1,0} = eΔV_DS with ΔV_DS = V_2 − V_1. Therefore, the period of peaks, ΔV_DS, corresponds to the subband separation of the channel.
body. From the \( g_0(V_{DS}) \) behavior in Figure 3b, we obtain \( \Delta E_{\text{int},1,0} \sim 65 \pm 10 \text{ meV} \) for the low-lying few subbands in the p-SiNW FET with cross section of 4.3 nm \( \times \) 5.7 nm. Remembering that the subband separation increases with the gate bias in a given channel body and is inversely proportional to the square of the channel radius,\(^{15} \) our experimental value of 65 \( \pm \) 10 meV is in accord with a theoretical prediction of \( \sim 50 \) meV for p-SiNW FET of 5 nm \( \times \) 5 nm cross section.\(^{20} \) For an order-of-estimation of subband separations in SiNWs, let us take a p-SiNW body as an infinitely confined cylindrical 1D electron system of radius \( r_0 \) treating gate oxide as an infinite potential barrier to Si channel body even though the valence-band offset of SiO\(_2\)-Si is \( \sim 4.5 \) eV.\(^{21} \) The lowest two subband separations \( \Delta E_{\text{int},1,0} \) are 58.1 and 53.1 meV if we use \( 2r_0 = 5 \) nm for NW diameter (71.8 and 66.5 meV if we use \( 2r_0 = 4.5 \) nm) and \( m^* = 0.15 \) \( m_0 \) of light-hole effective mass in the [110] direction, where \( m_0 \) is the free-electron mass. (See Supporting Information Text 3.) The lowest hole subband is of light holelike character.\(^{20} \) This order-of-magnitude estimation of intersubband separation is also in agreement with our experimentally extracted value (\( \Delta E_{\text{int},1,0} \sim 65 \pm 10 \text{ meV} \)) for low-lying subbands in our p-SiNW FET. This extracted subband separation at 300 K corresponds to \( \Delta E_{\text{int},1,0} \approx (1.7 \pm 0.24) k_B T \) or in terms of thermal energy to \( \Theta \approx 510 \pm 72 \) K, which is about one-half of the theoretical thermal broadening criterion (\( \Delta E \approx 3.5 k_B T \)) for clear resolution of quantum oscillations in mesoscopic transport measurements.\(^{2,22} \) Hence, the presence of measurable quantum oscillatory behavior in our p-SiNW FETs at room temperature is well justified.

Confinement-induced quantum oscillatory behavior is known to be observable provided that the source–drain bias \( V_{DS} \) is not much larger than subband separation \( \Delta E_{\text{int},1,0} \). For small \( V_{DS} \) nearly flat and parallel subband channels are expected to produce clear oscillations in source–drain transfer characteristics as far as \( eV_{DS} \) is not much larger than a few times the intersubband separation \( \Delta E_{\text{int},1,0} \).\(^{17} \) Under a strong source–drain bias field, the confinement potential is greatly tilted down along the channel by the drain bias such that the gate field can induce more carriers easily. When the chemical potential at the drain side \( \mu_D \) is pulled down drastically, the effective channel body length is significantly reduced and, as a result, the quantum mechanical interference effect can be visible in transport parameters such as conductance and mobility of short-length SiNW FETs in the quasi-ballistic regime.\(^{23,24} \) Park et al. also report enhanced drain current oscillations in inversion mode of their Si FET for high \( V_{DS} \) albeit at low temperature.\(^{25} \) (See Figure 3 in ref 25.) Nevertheless, the continuing (sometimes much enhanced) oscillatory behavior in \( \Delta I_{DS}/\Delta V_{BG} \) and \( g_0=\Delta V_{BG} \) at higher \( V_{DS} \) in our p-SiNW FETs is not fully understood yet. (See Supporting Information Figure S5.) One possible source of this observed effect could be related to strong electric field-induced intersubband scattering near the drain.\(^{26} \) We suppose that extremely nonequilibrium high field dielectric response would be responsible for the persisting oscillatory behavior at high drain–source electric field,\(^ {27} \) and more rigorous analysis such as nonequilibrium Green function approach to quantum transport equations\(^ {28} \) would provide microscopic understanding of carrier transport characteristics of such ultrathin quantum devices.

**Field-Effect Mobility Behavior of SiNW FETs.** Here, we identify quantum size effects in carrier mobility of p-SiNW FETs. Field-effect mobility (\( \mu \)) of conventional MOSFETs is written as \( \mu = (g_{DL})/(V_{DS}C_W) \), where \( L, W \), and \( C_W \) (\( \equiv C/(LW) \)) are the gate length, width, and the gate oxide capacitance per unit area, respectively. Therefore, mobility characteristics should also show oscillatory behavior with respect to gate voltage, similar to \( g_0 \) of the SiNW FETs. For reliable determination of \( C_W \), finite element mesh simulation was performed using COMSOL package with the specific geometry of each device, as measured by HR-TEM imaging.\(^ {11} \) Our simulated capacitance gives \( C_W \approx 4.0 \) mF/m\(^2 \). Mobility characteristics of p-SiNW FETs are shown in Figure 4 in terms of \( V_{BG} \) with \( V_{DS} = 50 \text{ mV} \) at 300 K. Figure 4a shows \( \mu \) of p-SiNW FETs for channel lengths of 2, 3, and 10 \( \mu m \). In obtaining the mobility curves shown in Figure 4, we used \( C = 4.15 \times 10^{-17} \text{ F}, 6.22 \times 10^{-17} \text{ F}, \) and \( 2.05 \times 10^{-16} \text{ F} \) for channel length 2, 3, and 10 \( \mu m \), respectively.

The mobility shows clear oscillatory behavior with \( V_{BG} \), similar to \( g_0 \). The periodic character of the 1D DOS is directly reflected as the periodic oscillation in carrier mobility of the SiNW FETs through the simple relation \( \mu \propto \tau \propto 1/DOS \), where \( 1/\tau \) is some effective scattering rate. Decrease (increase) in \( \mu \) with \( V_{BG} \) corresponds to increase (decrease) in the DOS. As the gate bias increases, gradual occupancy of additional subbands by carriers results in increase of drain current and the steepest current increase (and, hence, a mobility peak) occurs when a new subband channel opens up for carrier transport; the oscillatory behavior occurs when carriers must “wait” for the...
Fermi level in the channel to rise to include the subsequent subband. Figure 4a shows that peak mobility occurs at relatively low gate biases near $V_{BG} \sim 2$ V, and the overall mobility is enhanced in the NW devices with longer channel body. Although the NW device with 10 μm long channel body shows reduced transconductance behavior (as illustrated in Figure S2 in Supporting Information), it produces the highest peak mobility value, approaching over ~900 cm$^2$ V$^{-1}$ s$^{-1}$. This apparent feature is attributed to the fact that relative carrier mobility of various SiNW FETs is controlled by the product of $g_m (L/W)$, since the remaining factor, $V_{DS}C_{ox}$ in the expression $\mu = (g_m L)/(V_{DS}C_{ox} W)$ is independent of channel cross sectional dimensions; for example, $L/W$ is largest for the 10 μm long nanowire device due to long length and smallest NW cross section. The fact that $g_m$ does not scale proportionally with $(L/W)^{-1}$ implies an intrinsic increase of mobility in nanowires with a smaller cross section, like the 4.3 nm × 3.6 nm NW device in Figure 4a (also see Figure S2 in Supporting Information). Figure 4b shows field-effect mobility characteristics of 3 μm long SiNW FET with cross section of 4.3 nm × 5.1 nm and SiNB FET with cross section of 4.3 nm × 161 nm. The disparity in gate bias dependence of field-effect mobility in NW FETs as compared to NB FETs resembles the corresponding disparity in transport and transconductance characteristics of the two devices seen in Figure 2. (See also Figure S4 in Supporting Information.) The overall performance of SiNW and SiNB devices is distinctive due to the unique DOS of respective device. For the SiNB FET, the mobility continues to oscillate with $V_{BG}$ revealing uniformly spaced peaks, which is an indication of the ladderlike accumulated DOS profile of 2D subband channels. In contrast, mobility behavior of the SiNW FET discloses (more clearly at low gate bias fields) the behavior of inverse-square-root singularities at the bottoms of each 1D subband. At high gate bias, average mobility is considerably reduced in NW devices, as more subband channels are opened for carrier transport at higher gate bias, due to increased intersubband scattering caused by larger variation in effective mass of carriers in different subband.

Carry mobility can strongly be influenced by acoustic phonon scattering. The carrier-acoustic phonon scattering rate can be estimated employing deformation potential theory along with the Fermi golden rule. For a SiNW FET of 5 nm diameter and of $E_F = 10$ meV, we estimate the acoustic scattering time $\tau_{ac} \sim 8.7 \times 10^{-12}$ s at 300 K. (See Supporting Information Text 6.) Using $\tau_{ac} \sim 8.7 \times 10^{-12}$ s and $\nu_F = (2E_F/m^*)^{1/2} \sim 1.5 \times 10^8$ m/s, one can calculate the mean free path for carriers of light-hole mass to be $l_{ac} \sim 1.3$ μm. In sub-5 nm Si[110] NW FETs, the lowest two hole subbands are nearly two-fold degenerate light-hole-like, so that phonon-assisted intersubband scattering can be neglected within these two nearly degenerate subbands. Furthermore, considering Si Debye energy of 55 meV and significantly enhanced intersubband separation ($\Delta E_{sub} \sim 55–75$ meV) in sub-5 nm ultrathin SiNW FETs, acoustic phonon assisted intersubband scattering is expected to be rather minimal between the subsequent low-lying subband channels. All these features would clearly give rise to a boost in field-effect hole mobility in our p-SiNW FETs. Our observation is in line with theoretical predictions of enhanced hole mobility in strongly confined NWs. Since the carrier relaxation time is inversely proportional to the DOS, relaxation time $\tau(E)$ should also reveal oscillatory behavior because of the periodic inverse-square-root singular enhanced DOS at the 1D subband edges of the channel body. Although our analysis of carrier-acoustic phonon scattering rate is macroscopic, this estimation of low scattering rate is also in support of quantum oscillatory transport behavior (oscillatory behavior lends to high peak performance through unique DOS) in our sub-5 nm SiNW FETs persisting at room temperature. Surface roughness scattering could potentially be significant in such small nanowires. However, we expect it to be minimal because thermal oxidation on plasma etched NWs evidently reduces sidewall roughness. Furthermore, as these FETs are back-gated, the carriers would be confined away from the possibly imperfect top oxide-Si interface. Impurity scattering is expected to be negligible due to low doping and reduced volume of ultrathin nanowire devices. We suppose the carriers are physically scattered mostly at the metallic source and drain contacts in our junctionless devices. Additionally, reduced carrier effective mass in an ultrathin SiNW channel body also constitutes enhanced performance (through reduced acoustic phonon assisted intersubband carrier scattering) for transport within the SiNW FETs.

In summary, we have presented evidence of confinement-induced quantum oscillatory behavior prevailing at 300 K in drain–source current, transconductance, and field-effect mobility characteristics of ultrathin top-down fabricated SiNW FETs. Effects of quantum confinement on channel conductance and transconductance are described in terms of quantized 1D subband structures and the corresponding unique 1D DOS. Carrier mobility characteristics are shown to differ depending on the cross sectional geometry of the channel body, such that disparity in mobility characteristics of SiNW and SiNB devices resemble the corresponding disparity in transfer conductance characteristics of the drain–source current.

We conclude that strongly enhanced peak field-effect mobility in p-SiNW FETs results from the unique 1D DOS of inverse-square-root singularity. Ambient operation of SiNW devices with cross sectional dimensions of sub-5 nm scales should be understood in terms of quantum aspects of strongly confined carriers. As such, this study would serve as a guide for basic understanding of physical characteristics of nanoelectronics devices consisting of ultrathin SiNW FETs as potential key building blocks for future electronics devices. We believe quantum confinement effects are a key avenue to unlock performance and extend scalability of future Si technology as well as foster new applications of Si devices.33

ASSOCIATED CONTENT

Supporting Information

Additional information regarding (1) carriers in confined structures, (2) channel length- and width-dependences of transfer characteristics, (3) intersubband separations in cylindrical nanowires, (4) channel conductance behavior with the gate- and channel-bias voltages, (5) subband spectroscopy, and (6) carrier-acoustic phonon scattering rate and mean free path. This material is available free of charge via the Internet at http://pubs.acs.org.

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